Self-aligning silicon interposer tiles and silicon bridges for large nanophotonics enabled systems

H.S. Yang, C. Zhang and M.S. Bakir

A two-and-a-half-dimensional (2.5D) platform for enabling silicon nano-photonics and dense electrical interconnections between interposers in a tile-like configuration is presented. Three 20 × 20 mm silicon interposer tiles are assembled directly on an FR4 printed wiring board (PWB), and two 6 × 20 mm silicon bridges are assembled on top of the interposer tiles. Accurate alignment of interposer tiles to bridges, an important metric in enabling highly efficient optical coupling, is provided using positive self-alignment structures (PSASs). It is demonstrated that by using PSAS on two silicon substrates, sub-micron alignment between substrates is possible; in the cascaded configuration involving FR4, <5 μm alignment accuracy is obtained. In addition, electrical interconnection via a bridge using mechanically flexible interconnects (MFIs) is demonstrated, which made non-bonding interconnections from one interposer tile to another via a silicon bridge, allowing silicon bridges as well as the interposer tiles to be replaced. Total silicon interposer area available is 960 mm^2.

Introduction: The need for high-bandwidth and low-energy interconnections has been on the rise, as the demand for high-performance systems continues to grow. To that end, the interconnect limitations within a module is being addressed through the use of a silicon interposer (i.e. two-and-a-half-dimensional (2.5D)) and 3D integrated ICs. However, technologies to interconnect two modules remain limited; the current solution for electrical interconnection is to use the low-performance wires on printed wiring board (PWB), whereas the solution for optical interconnection requires the use of optical fibres, which makes scaling difficult.

Our vision (Fig. 1) is a wafer-level batch fabricated platform, where nanophotonics can be leveraged in providing module-to-module interconnections; silicon bridges are placed on top of two or more interposer 'tiles' to provide a silicon-based link. The silicon-based link enables the use of nanophotonic devices such as the grating coupler and waveguides to be fabricated both on the tiles and the bridges [1]. Accurate alignment needed for efficient optical coupling [2] is provided by positive self-alignment structures (PSASs), which self-align the motherboard, tiles and bridges. The motherboard-to-tile and the tile-to-bridge electrical interconnections are provided using mechanically flexible interconnects (MFIs); the large vertical range of motion allows non-planarity of the motherboard surface to be compensated for.

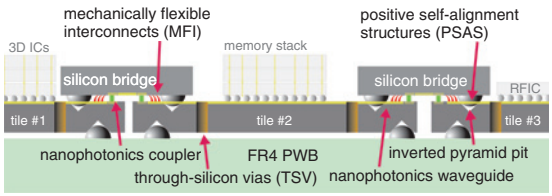

Fig. 1 *Direct mounting of silicon interposers on FR4 PWB using PSASs and MFIs*

In this Letter, we present the first significant milestone in demonstrating the key features of the platform that utilises two interconnect and packaging technologies: accurate passive alignment of PWB, tiles and bridges using PSASs; and tile-to-bridge electrical interconnections using MFIs.

Positive self-alignment structures: The PSASs and inverted pyramid pits (Fig. 2) enable accurate alignment of a silicon substrate and an arbitrary substrate (including FR4, ceramic and glass), without an accurate placement tool. Multiple PSAS/pit pairs are placed near the edges of the tiles or bridges, and as PSASs, which have been precisely reflowed, are guided towards the centres of the inverted pyramid pits, initial misalignment as much as 150 μm can be consistently corrected; for silicon to silicon alignment, up to 1 μm alignment accuracy has been demonstrated [3], whereas for silicon to FR4 substrate alignment, consistent accuracy of <5 μm is possible. To maintain the alignment, a clamping mechanism is required so that all PSAS and pits remain engaged (adhesives were used in this work).

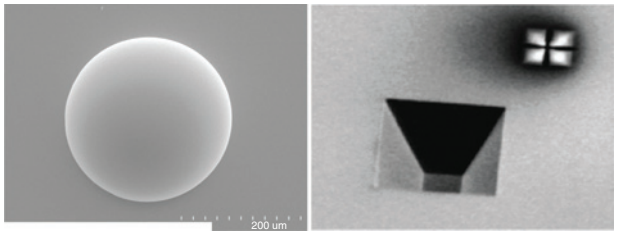

Fig. 2 *SEM image showing PSASs and pit*

In the work described in this Letter, four PSAS per interposer tiles are fabricated on the PWB. This is done by patterning a 95 μm photoresist (AZ 40XT-11D) layer and reflowing the resulting cylindrical structure to form semi-spheres. Four PSAS are also fabricated on each of the silicon bridges. PSAS fabrication process is CMOS compatible; the maximum temperature involved is 150°C. Additionally, anisotropically etched pits are fabricated on both sides of the interposer tiles; the pits on the side facing the PWB corresponds to PSAS on the PWB, whereas the pits on the side facing the top correspond to the PSAS on the silicon bridges (Fig. 3).

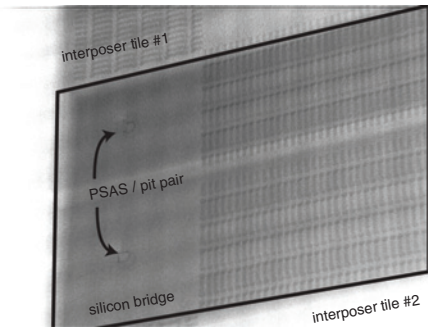

Fig. 3 *X-ray imaging showing two aligned pit/PSAS pairs, silicon bridge and two interposer tiles*

Array of MFIs, as well as traces connecting them on both interposer tiles and silicon bridge are shown

Mechanically flexible interconnects: MFIs are highly compliant structures designed to maximise the elastic vertical range of motion [4]. This mechanical property enables a substrate containing MFIs to form temporary electrical connections with pads on another substrate, and it is a key enabler in allowing interposer tiles and silicon bridges to be replaced as well. As the tip end of the MFI is not bonded, it is free to slide. As such, the CTE (coefficient of thermal expansion) mismatch between two layers can be compensated for without significant lateral deformation of the MFIs. Thus, the design of the MFI focused on maximising the vertical range of motion. In this demonstration, MFIs are used to electrically interconnect (power and signal) multiple interposer tiles and have been modified to address new challenges associated with temporary interconnectivity (Fig. 4):

- pointy tip replaces the circular solder pad area for improved contact resistance;
- structure points upwards to ensure that the contact with the pad is made at the tip end; and
- optimised shape ensures that the tip end remains in contact with the pad when deformed vertically.

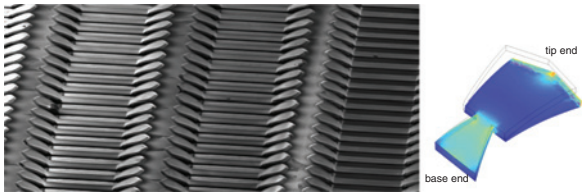

Fig. 4 *SEM of MFIs show pointy tip end of structure (left)*

Bending profile of MFI design ensures that vertical range in which tip remains highest point is maximised (right)

Assembly of interposer tiles and Si bridges: After the fabrication of PSAS, pits and MFIs, interposer tiles are brought together and coarsely aligned to the PWB. Then, the interposer tiles are gently pushed downwards and slightly moved around laterally until all PSAS and pit pairs engage and interposer tiles become fixed. The height of the PSAS is larger than the height of the MFIs; this prevents damage to the MFIs during the described self-alignment process. Silicon bridges are assembled in a similar manner. Properties of the assembled platform are shown in Table 1.

Table 1: Summary of properties for assembled platform

Properties	Values
Interposer tile area (cm^2)	4.0
Number of interposer tiles	3
Silicon bridge area (cm^2)	1.2
Number of silicon bridge	2
Number of MFI I/Os per tiles/bridge interface	2000
Total available silicon interposer area (cm^2)	9.6

In this work, an adhesive material is applied at the edges of the interposer tiles and the silicon bridges to hold the assembly. Future work will involve clamping mechanisms which will allow tiles and bridges to be replaced and reassembled repeatedly. The assembled interposer tiles and silicon bridges are shown in Fig. 5. The measurement of the alignment accuracy before and after the application of the adhesive material shows that the alignment is not affected.

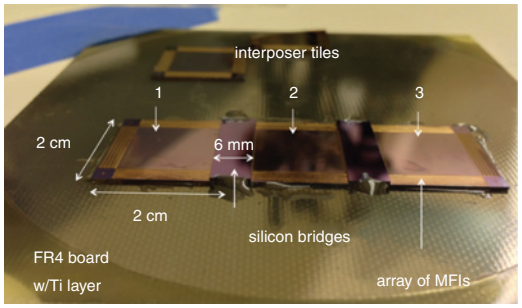

Fig. 5 *Photograph of three interposer tiles mounted directly on PWB, and interconnected using silicon bridges and MFIs*

The expected vertical spacing between interposer tiles and silicon bridges, and between interposer tiles and PWB, can be calculated via simple geometrical calculations. As such, contact with MFIs after the self-alignment process can be assured, and the amount of vertical deformation and the force applied by the tip end of the MFIs can also be determined. ANSYS FEM (finite-element modelling) simulation shows that MFI deformations remain in the elastic regime.

Alignment accuracy measurement: Accurate alignment between the interposer tiles and the silicon bridge is required in ensuring that efficient coupling is achieved for optical and electrical communication. The alignment accuracy also determines the minimum size of the interface inputs–outputs (I/Os).

Since the silicon bridges are aligned to the interposer tiles with an assumption that interposer tiles are aligned perfectly to PWB, it is essential that the alignment between PWB and interposer tiles is accurate, even though nanophotonics and high-density I/Os do not exist between those two layers. The alignment accuracy is measured by observing the vernier patterns fabricated on the silicon bridge and the interposer tiles via infrared microscopy. The alignment results are summarised in Table 2.

Table 2: Misalignment between silicon bridge and interposer tiles

	Silicon bridge 1		Silicon bridge 2	
Regions	Horizontal (μm)	Vertical (μm)	Horizontal (μm)	Vertical (μm)
Bottom left	−4.0	+4.6	−5.2	−5.0
Bottom right	−5.4	−4.8	−5.0	−5.0
Top right	+5.8	+3.2	−5.8	−5.2
Top left	+6.0	−5.0	−7.6	−5.0

Electrical measurements: Electrical resistance is measured between interposer tiles to verify electrical connectivity. To form a daisy chain, 20 MFIs per silicon bridge are interconnected in series and 100 such daisy chains exist, which results in 2000 MFIs per silicon bridge. The results are summarised in Table 3. Expected values are calculated by taking into account the resistance of MFIs measured using the four-probe measurement, as well as the wire traces fabricated on the interposer tiles and silicon bridges.

Table 3: Resistance between interposer tiles

	Resistance between tiles through bridge		
	1 and 2	2 and 3	1 and 3
Average (Ω)	1.51	1.59	4.98
Expected value (Ω)	1.32	1.32	4.36
Standard deviation (Ω)	0.138	0.140	0.363
Number of measurements	20	20	20
Number of MFIs in chain	20	20	40

Conclusion: A novel platform for interconnecting silicon interposer tiles via silicon bridges is proposed. PSAS ensure accurate alignment between PWB, interposer tiles and silicon bridges to accommodate high-density I/Os and nanophotonics communication between interposer tiles, whereas PSAS and MFI's non-bonding nature of the assembly process allows individual interposer tiles to be replaced for increasingly large and complex systems.

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One or more of the Figures in this Letter are available in colour online.

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